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EXAMINER

HSU, JONI

ART UNIT PAPER NUMBER

2628

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/726,220	Applicant(s) FOULADI ET AL.	
	Examiner Joni Hsu	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-54 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14, 16-23, 25, 27-35, 37, 39, 40, 43-51, 53 and 54 is/are rejected.
- 7) ☒ Claim(s) 13, 15, 24, 26, 36, 38, 41, 42 and 52 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's arguments filed September 22, 2006 have been fully considered but they are not persuasive.

2. With regard to Claim 1, Applicant argues that queues 50a, 50c, 50e, 50d, 50g and 50j are part of interface controller 14, and are not described or illustrated in Chin (US006202101B1) as being part of the memory controller 44 (page 12, paragraph 8).

In reply, the Examiner points out that the memory controller 44 in Chin (*memory controller 44 arbitrates*, Col. 8, lines 56-62) is considered to be equivalent to the arbitration control (825, Figure 8) of the present invention. The interface controller 14 in Chin (*bus interface unit provides an interface between components clocked at similar rates, bus interface unit 14 contains a memory controller*, Col. 7, lines 27-31) is considered to be equivalent to the memory controller (Figure 8) of the present invention. Therefore, the queues in Chin are part of the memory controller.

Applicant argues that the configuration shown in Figure 6 (including queue 68) is described in Chin as being part of the processor controller 42, not memory controller 44 (page 13, paragraph 3).

In reply, the Examiner points out that Chin teaches that the processor controller 42 is part of the interface controller 14 (Col. 8, lines 23-26), which is equivalent to the memory controller, as discussed above. Therefore, queue 68 is part of the memory controller.

Applicant argues that memory request queue 68 of Chin stores requests “dispatched on the processor bus,” not requests from a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources (page 13, paragraph 4). Applicant argues that because queue 68 of Chin does not receive information from a plurality of buffer memories, Chin does not suggest a control circuit involved in transferring information as claimed (page 13, paragraph 5).

In reply, the Examiner points out that Chin teaches that memory request queue 68 is coupled to the plurality of buffer memories (queues) for storing requests for main memory access from each of the plurality of resources (processors) (*temporarily stored within a M2P queue 50c*, Col. 12, lines 65-67; *type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or sent to M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64*, Col. 13, line 51-Col. 14, line 5), as recited in the claims, and therefore suggests a control circuit involved in transferring information.

Applicant argues that Queue 50c is unrelated to the concept of controlling a transfer of information from buffer memories to a multiple resource buffer as claimed (page 13, paragraph 6). Chin describes queues that involve requests from the processor bus, not from a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources requesting memory access (page 14, paragraph 1).

In reply, the Examiner disagrees. Chin discloses that the memory request will access a memory location and data at that location is temporarily stored within an M2P queue 50c (Col.

12, lines 65-67). The type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or set to M2P or P2M (attributed to memory data queue). The memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64 (Col. 13, line 51-Col. 14, line 5). The M2P queue 50c is a buffer memory and the memory request queue is a multiple resource buffer. Since the system has a means for using an in-order queue to control whether the data is to be drawn from the M2P queue and the memory request queue snoops the results maintained in the in-order queue, this means that there is a means for controlling a transfer of information from the M2P queue 50c (buffer memory) to the memory request queue (multiple resource buffer), and therefore Queue 50c is related to this concept. Since the memory request will access a memory location and data at that location is temporarily stored within a M2P queue 50c (Col. 12, lines 65-67), and there are a plurality of these queues (Col. 8, lines 30-37), Chin discloses a plurality of queues (buffers) each of which is operatively coupled to one of the plurality of resources (processors) requesting memory access.

3. With regard to Claim 14, Applicant argues that queue 50c of Chin is not a write request queue and there is no suggestion in Chin of initiating the flushing of a resource's write request queue when the resource is writing to main memory (page 14, paragraph 7).

In reply, the Examiner disagrees. Chin discloses that the memory request will access a memory location and data at that location is temporarily stored within an M2P queue 50c (Col. 12, lines 65-67), and therefore queue 50c is a write request queue. Chin discloses a de-queuing

operation for queue 50c (Col. 13, lines 1-11), and therefore Chin discloses initiating the flushing of a resource's write request queue when the resource is writing to main memory.

4. Applicant argues that the Examiner rejected Claim 16 under the same rationale as Claim 1, but Claim 1 does not specifically set forth the same limitations as Claim 16 (page 15, paragraph 2).

In reply, the Examiner has more explicitly rejected Claim 16 below.

5. Applicant argues that the Examiner rejected Claim 27 under the same rationale as Claim 1, but Claim 1 does not specifically set forth the same limitations as Claim 27 (page 15, paragraph 6).

In reply, the Examiner has more explicitly rejected Claim 27 below.

Applicant argues that neither Chin nor Harriman (US006092158A) disclose steps of storing requests in first and second queues and delaying forwarding requests (page 16, paragraph 2).

In reply, the Examiner disagrees. Chin discloses storing requests in first and second queues (Col. 8, lines 30-37; Col. 12, lines 65-67). Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*, Col. 1, lines 35-50), and therefore delays forwarding requests.

6. Applicant argues that the Examiner rejected Claim 40 under the same rationale as Claim 14, but Claim 14 does not specifically set forth the same limitations as Claim 40 (page 16, paragraph 5).

In reply, the Examiner has more explicitly rejected Claim 40 below.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-7, 14, 16-18, 25, 27-30, 37, 39, 40, 43-46, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) in view of Harriman (US006092158A).

10. With regard to Claim 1, Chin discloses in a graphics system including a main processor (12, Figure 1) and a graphics processing system (20) for generating graphics images on a display in cooperation with the main processor (Col. 1, lines 56-59; *CPU bus connects a CPU 12 to a bus interface unit 14, interface unit 14 may also include a graphics port to allow communication to a graphics accelerator 20*, Col. 7, lines 21-37), and a main memory (18), the system including a plurality of resources (40, 42, 46, Figure 2) requesting access to the main memory, a memory controller comprising a plurality of buffer memories (50a, 50c, 50e, 50d, 50g, 50j, Figure 2), each of the buffer memories being operatively coupled to one of the plurality of resources requesting access to the main memory for storing information indicative of a request for main memory access (Col. 8, lines 20-37). The memory controller 44 in Chin (*memory controller 44 arbitrates*, Col. 8, lines 56-62) is considered to be equivalent to the arbitration control (825, Figure 8) of the present invention. The interface controller 14 in Chin (*bus interface unit provides an interface between components clocked at similar rates, bus interface unit 14 contains a memory controller*, Col. 7, lines 27-31) is considered to be equivalent to the memory controller (Figure 8) of the present invention. Therefore, the queues in Chin are part of the memory controller. Chin discloses a multiple resource buffer memory (memory request queue 68, Figure 6) coupled to the plurality of buffer memories for storing requests for main memory access from each of the plurality of resources; and a control circuit for controlling the transfer of information from the plurality of buffer memories to the multiple resource buffer memory (*temporarily stored within a M2P queue 50c*, Col. 12, lines 65-67; *type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or sent to*



*M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64, Col. 13, line 51-Col. 14, line 5).* Chin teaches that the processor controller 42 is part of the interface controller 14 (Col. 8, lines 23-26), which is equivalent to the memory controller. Therefore, queue 68 is part of the memory controller. Chin teaches that memory request queue 68 is coupled to the plurality of buffer memories (queues) for storing requests for main memory access from each of the plurality of resources (processors) *(temporarily stored within a M2P queue 50c, Col. 12, lines 65-67; type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or sent to M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64, Col. 13, line 51-Col. 14, line 5),* and therefore suggests a control circuit involved in transferring information. Chin discloses that the memory request will access a memory location and data at that location is temporarily stored within an M2P queue 50c (Col. 12, lines 65-67). The type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or set to M2P or P2M (attributed to memory data queue). The memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64 (Col. 13, line 51-Col. 14, line 5). The M2P queue 50c is a buffer memory and the memory request queue is a multiple resource buffer. Since the system has a means for using an in-order queue to control whether the data is to be drawn from the M2P queue and the memory request queue snoops the results maintained in the in-order queue, this means that there is a means for controlling a transfer of information from

the M2P queue 50c (buffer memory) to the memory request queue (multiple resource buffer), and therefore Queue 50c is related to this concept. Since the memory request will access a memory location and data at that location is temporarily stored within a M2P queue 50c (Col. 12, lines 65-67), and there are a plurality of these queues (Col. 8, lines 30-37), Chin discloses a plurality of queues (buffers) each of which is operatively coupled to one of the plurality of resources (processors) requesting memory access.

However, Chin does not disclose the means to reduce the frequency of switching from main memory write operations to main memory read operations. However, Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*, Col. 1, lines 35-50) similar to instant claim limitation "to reduce the frequency of switching from main memory write operations to main memory read operations".

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Chin to include the means to reduce the frequency of switching from main memory write operations to main memory read operations as suggested by Harriman because it results in an improved and optimized overall memory access performance.

11. With regard to Claim 2, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues (Col. 8, lines 20-37).

12. With regard to Claim 3, Chin discloses that the multiple resource buffer memory (68, Figure 4) is a main memory write queue (Col. 11, lines 9-20).

13. With regard to Claim 4, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues (Col. 8, lines 20-37), and wherein the multiple resource buffer memory (68, Figure 6) is a main memory write queue (Col. 11, lines 9-20), and wherein the control circuit (44, Figure 2) is operable to control the rate at which write requests are coupled to the multiple resource buffer memory from the plurality of buffer memories (*Memory controller 44 arbitrates among processor write, processor reads, peripheral writes, peripheral reads and refresh. Arbitration for each cycle is pipelined into the current memory cycle which ensures that the next memory address is available on the memory bus before the current cycle is complete*, Col. 8, lines 52-67; Col. 13, line 51-Col. 14, line 5).

14. With regard to Claim 5, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues and further including a plurality of main memory read queues (50c, 50d, 50j), each read queue being operatively coupled to a resource (40, 42, 46) requesting to read information from the main memory (18, Figure 1) (Col. 8, lines 20-37).

15. With regard to Claim 6, Chin describes that the control circuit (44, Figure 2) includes arbitration circuitry for arbitrating requests for access to the main memory (18, Figure 1) (Col. 8, lines 56-62).

16. With regard to Claims 7, 18, 30, and 46, Chin describes that the arbitration circuitry is operable to control the frequency with which the requesting resources are enabled to participate in the arbitrating for main memory access (Col. 8, lines 56-67).

17. With regard to Claims 14, 25, and 37, Chin discloses that the plurality of buffer memories (50a, 50c, 50e, 50d, 50h, 50g, 50j, Figure 2) and the multiple resource buffer memory (68, Figure 5) are write request queues (Col. 8, lines 20-37; Col. 11, lines 9-20), and wherein a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue (de-queuing, Col. 13, lines 1-11). Chin discloses that the memory request will access a memory location and data at that location is temporarily stored within an M2P queue 50c (Col. 12, lines 65-67), and therefore queue 50c is a write request queue. Chin discloses a de-queuing operation for queue 50c (Col. 13, lines 1-11), and therefore Chin discloses initiating the flushing of a resource's write request queue when the resource is writing to main memory.

18. With regard to Claim 16, Chin discloses in an information processing system including a main processor (12, Figure 1; 42, Figure 2), a main memory (18, Figure 1), and at least a first (40, Figure 2) and a second resource (46) competing with the main processor for access to the main memory (Col. 1, lines 56-59; Col. 7, lines 21-37; Col. 8, lines 20-37), a memory controller (14) comprising a main processor related interface including a main processor read request queue (50c) and a main processor write request queue (50a); a first resource related interface including at least one of a first resource read request queue (50d) and a first resource write request queue

(50e); a second resource related interface including at least one of a second resource read request queue (50h) and a second resource write request queue (50g) (Col. 8, lines 20-37); a multiple resource write request queue (memory request queue 68, Figure 6) for receiving requests for writing to the main memory; and a memory access control circuit for granting access to the main memory, the memory access control circuit being coupled to receive read requests from each of the read request queues and for receiving write requests from the multiple resource write request queue (Col. 12, lines 65-67; Col. 13, line 51-Col. 14, line 5).

19. With regard to Claim 17, Claim 17 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

20. With regard to Claims 27 and 43, Chin discloses in an information system including a main processor (12, Figure 1), a main memory (18), and at least a first (40, Figure 2) and a second resource (46) competing with the main processor for access to the main memory (Col. 1, lines 56-59; Col. 7, lines 21-37; Col. 8, lines 20-37), a method of controlling access to the main memory comprising the steps of storing requests for main memory access from a first resource in a first resource request queue (50d, 50e); storing requests for main memory access from a second resource in a second resource requests queue (50h, 50g) (Col. 8, lines 20-37); and granting requests for main memory access by the memory access control circuit (Col. 12, lines 65-67; Col. 13, line 51-Col. 14, line 5).

However, Chin does not teach delaying forwarding requests for main memory access to a memory access control circuit to reduce the frequency of switching between memory read states

and memory write states. However, Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*, Col. 1, lines 35-50) similar to instant claim limitation "delaying forwarding requests for main memory access to a memory access control circuit to reduce the frequency of switching between memory read states and memory write states". This would be obvious for the same reasons given in the rejection for Claim 1.

21. With regard to Claim 28, Chin discloses storing requests in a multiple resource write queue (68, Figure 4; Col. 11, lines 9-20).

22. With regard to Claim 29, Claim 29 is similar in scope to Claim 28, and therefore is rejected under the same rationale.

23. With regard to Claims 39 and 53, Chin discloses that the step of granting requests includes the step of fulfilling requests for main memory access in the order requested (*maintains prior ordering of data sent to and returned from the memory*, Col. 1, lines 9-15).

24. With regard to Claim 40, Chin discloses in an information system including a main processor (12, Figure 1), a main memory (18), and at least a first (40, Figure 2) and a second resource (46) competing with the main processor for access to the main memory (Col. 1, lines 56-59; Col. 7, lines 21-37; Col. 8, lines 20-37), a method of controlling access to the main

memory comprising the steps of storing requests for writing to the main memory from a first resource in a first resource write request queue (50d, 50e); writing to main memory by the first resource (Col. 8, lines 20-37); generating a write queue flush signal by the first resource to initiate copying information in the first resource write request queue to main memory; and flushing the first resource write request queue (de-queuing, Col. 13, lines 1-11).

25. With regard to Claims 44, 45, and 54, these claims are similar in scope to Claims 28, 29, and 1 respectively and therefore are rejected under the same rationale.

26. Claims 8-12, 19-23, 31-35, and 47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) and Harriman (US006092158A) in view of Jeddeloh (US006330647B1).

27. With regard to Claims 8, 19, 31, and 47, Chin and Harriman are relied upon for the teachings as discussed above relative to Claim 1.

However, Chin and Harriman do not teach a memory access control register associated with one of the resources, wherein the control circuit includes arbitration circuitry responsive to the contents of the memory access control register for determining the frequency that the resource is permitted to participate in the arbitrating for main memory access. However, Jeddeloh discloses an arbiter 210 in combination with configuration registers 214 to record access count values for each requestor (resources or class of requester) and counters 214 may be

used by arbiter 210 to track the number of memory access operations remaining for a selected requester (Col. 3, lines 53-67; Col. 4, lines 1-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Chin and Harriman to include a memory access control register associated with one of the resources, wherein the control circuit includes arbitration circuitry responsive to the contents of the memory access control register for determining the frequency that the resource is permitted to participate in the arbitrating for main memory access as suggested by Jeddeloh because it provides for efficient memory access control without denying access to those requestors issuing single access transactions and/or low priority requests for an unacceptable long time (Col. 1, lines 48-51).

28. With regard to Claims 9, 20, 32, and 48, Chin does not teach a set of control registers, the control registers being programmable by the main processor. However, Jeddeloh discloses the control registers (configuration registers 212) being programmable by the main processor (system controller 102) (*system controller 102...may...set and adjust requestor access count values... (i.e., modify values stored in configuration register 212*, Col. 5, lines 1-10). This would be obvious for the same reasons given in the rejection for Claim 8.

29. With regard to Claims 10, 21, 33, and 49, Chin discloses that the control circuitry (44, Figure 2) is operable to arbitrate between the resources for granting requests for main memory access (Col. 8, lines 56-62).



However, Chin does not teach wherein the control registers include a plurality of memory bandwidth control registers which are accessed by the control circuitry in determining which resource will be granted main memory access. However, Jeddeloh discloses implicitly, wherein the control registers include a plurality of memory bandwidth control registers which are accessed by the control circuitry in determining which resource will be granted main memory access (*count values may be determined dynamically at...system start up and/or modified during system operations...access count values may be based on requestor operating speed, wherein faster devices are allocated larger access count values*, Col. 5, lines 1-10). This would be obvious for the same reasons given in the rejection for Claim 8.

30. With regard to Claims 11, 22, 34, and 50, Chin does not teach that each of the memory bandwidth control registers is respectively associated with a resource seeking main memory access. However, Jeddeloh discloses wherein each of the memory bandwidth control registers (configuration registers 212) is respectively associated with a resource seeking main memory access (*configuration registers 212 may be used to record access count values for each requestor (or class of requestor)*, Col. 4, lines 1-6). This would be obvious for the same reasons given in the rejection for Claim 8.

31. With regard to Claims 12, 23, 35, and 51, Chin does not teach that the control registers include at least one register associated with a main memory access requesting resource for storing data for the requesting resource indicative of at least one of memory usage and memory bandwidth for that resource. However, Jeddeloh discloses implicitly at least one register for the

requesting resource indicative of at least one of memory usage and memory bandwidth for that resource (*configuration registers 212 may be used to record access count values...counters 214 may be used by arbiter 210 to track number of memory access operations*, Col. 4, lines 1-6). This would be obvious for the same reasons given in the rejection for Claim 8.

### ***Allowable Subject Matter***

32. Claims 13, 24, 36, and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art fails to particularly disclose a register indicative of wasted memory cycles due to granting memory access to that resource.

33. Claims 15, 26, 38, 41, and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

  
ULKA CHAUHAN  
SUPERVISOR  
PATENT EXAMINER